# PATENT ABSTRACTS OF JAPAN

(54) DIGITAL SIGNAL PROCESSING CIRCUIT FOR SOUND FIELD CONTROL

(57)Abstract:

PURPOSE: To obtain a circuit without extending a hardware scale when plural sampling frequencies are handled in a digital signal processing system for sound field control.

CONSTITUTION: A storage area designation code s8 converted from a recognition code s4 is inputted to the address decoder 4d of a coefficient memory circuit 4. When the code shows '00', a storage area 4a is designated, and fixed coefficient data s9 in accordance with the sampling frequency fs1 is outputted sequentially according to sequence data s7 from a sequence memory circuit 5. When the code shows '01', a storage area 4b is designated, and the data s9 in accordance with the sampling frequency fs2 is outputted. When the code shows '10', a storage area 4c is designated, and the data s9 in accordance with the sampling frequency fs3 is outputted. An arithmetic circuit 1 receives the fixed coefficient data s9 and serial data s10 from a serial data memory circuit 6, and performs an arithmetic operation.
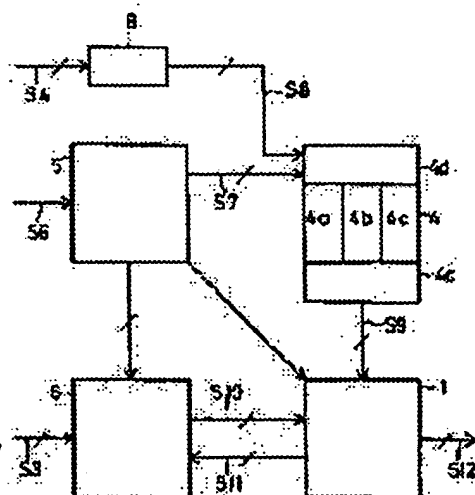
LEGAL STATUS

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the digital digital disposal circuit for sound field control.
[0002]
[Description of the Prior Art] Generally it is calling it sound field control to acquire an ambient atmosphere as if it was in the theater or the concert hall by domestic or the automatic in the car one. The general technique of this sound field control is making a surround signal from the audio signal of two channels. There is the technique of having used digital signal processing for the means which makes this surround signal.
[0003] Since CD (compact disk) appeared in 1982, digital Ore DIOSO-SU is increasing. For example, they are DAT (digital audio tape recorder), BS (satellite broadcasting service), VD (videodisk player), etc. The data transmission between devices is possible for these DEJITARUSO-SU by the digital audio interface. By this, while having a digital input, the amplifier equipped with the D/A conversion circuit has appeared. According to this, compared with what was transmitting the audio signal between devices by the analog transmission, reduction of an external noise and reduction of tone-quality degradation accompanying various kinds of analog signal processings are possible.
[0004] By the way, Dolby surround is in one of the methods which acquires a surround signal from the audio signal of two channels. This Dolby surround is a sound system for movies, and will appear in 1975. The audio signal of a total of four channels of one back is encoded to two channels at the three-channel list of the center of the front, the front left, and the front right, the decoder of dedication memorizes in the sound track of a motion-picture film, and this restores four at the time of encoding at the time of playback. And the Dolby prologic decoder (indicated by JP,61-251400,A for details.) which takes the same configuration as a movie theater appeared in 1987. Ahead [two], this decoder cancels the trouble that an image and an image shift as a right-and-left loudspeaker separates.
[0005] A Dolby prologic decoder is usually constituted from a detector circuit, an adder circuit, a VCA (armature-voltage control amplifier), etc. by the filter circuit and list which used analog components, such as an analog arithmetic element and a capacitor, and resistance. And signal processing, such as input-level automatic amendment, directivity emphasis, and channel control, is performed. In the above-mentioned analog circuit, the filter which has various kinds of time constants is contained, and these time constants must be settled in a predetermined specification. When performing signal processing (usually analog signal processing) in this Dolby prologic decoder in digital signal processing, they are the audio signal Lt of two channels, and Rt. It is expressed by carrying out A/D conversion with a predetermined sampling frequency by the digital data (usually PCM data) sampled and quantized.
[0006] When it constitutes signal processing systems for sound field control, such as the above-mentioned Dolby prologic decoder, using digital signal processing, there is an IIR (Infinite Impulse Response) digital filter as an operation system which is to the base in the case of performing processing. Hereafter, it explains taking the case of a secondary IIR filter (BAIKADDO filter). Transfer function of a

secondaryIIR filter "H (z)" H (z) =(a0+a1*z-1+a2*z-2)/(1-b1*z-1-b2*z-2)
It becomes. It is here and is z=exp (-jomegaTs).
omega=2pif ("f" is an analog frequency)
Ts =1/fs ("fs" is a sampling frequency)
It is j2 =-1. Moreover, the configuration of this secondaryIIR filter is shown in drawing 5 . As shown in
an upper type, when a sampling frequency "fs" changes, the value of "H (z)" in a certain specific analog
frequency will change with change of "z=exp (-jomegaTs)." That is, in order to keep "H (z)" the same to
two or more sampling frequencies "fs", each fixed factor (filter factor) "a0" of an upper type, "a1", "a2",
"b1", and "b2" must be changed. Therefore, in order [three kinds of] to make it correspond to "fs" (fs1,
fs2, fs3) fixed factor corresponding to fs1 : a01, a11, a21, b11, fixed factor corresponding to b21fs2 :
a02, a12, a22, b12, fixed factor corresponding to b22fs3 : Three fixed factor sets of a03, a13, a23, b13,
and b23 are needed.
[0007] Above, when digital signal processing performs a signal processing system for sound field
control like the Dolby prologic decoder currently conventionally performed mainly by analog signal
processing, it is necessary to determine a fixed factor (filter factor) like, depending on a sampling
frequency. Thus, when performing digital signal processing to two or more sampling frequencies, two or
more signal processors are prepared corresponding to each sampling frequency, and, generally the
method of switching those equipments according to each sampling frequency, and obtaining an
operation output is considered.
[0008]
[Problem(s) to be Solved by the Invention] However, by the above-mentioned conventional approach, in
order to have to prepare two or more signal processors corresponding to each sampling frequency, there
was a trouble that the scale of hardware became large.
[0009] In the digital signal processing system for sound field control, the purpose of this invention is
offering the circuit which can be constituted, without increasing a hardware scale, when dealing with
two or more sampling frequencies.
[0010]
[Means for Solving the Problem] In the digital digital disposal circuit for sound field control which this
invention carries out digital data processing of the audio signal of two channels by which the analog to
digital was carried out in arithmetic circuits, such as a digital filter, and acquires the digital output signal
of three or more channels The digital data corresponding to the fixed factor in the transfer function of a
digital filter is memorized to two or more storage regions corresponding to two or more sampling
frequencies which can be set in the above-mentioned analog-to-digital actuation. The multiplier store
circuit where two or more above-mentioned storage regions are specified corresponding to the
discernment data which identify two or more above-mentioned sampling frequencies, C KENSUDE-TA
which reads the above-mentioned fixed factor memorized in the above-mentioned storage region is
memorized, and it is characterized by having the sequence store circuit which reads the above-
mentioned fixed factor by this C KENSUDE-TA.
[0011]
[Example] Drawing 1 and drawing 2 are the block diagrams having shown the system containing the
digital digital disposal circuit for sound field control. What is necessary is not to be limited to this, of
course, to carry out digital data processing of the audio signal of two channels by which the analog to
digital was carried out in arithmetic circuits, such as a digital filter, and just to acquire the digital output
signal of three or more channels as a digital digital disposal circuit for sound field control, although a
Dolby prologic decoder (a configuration equivalent to this is constituted in digital one here although the
decoder indicated by JP,61-251400,A etc. is said.) can be raised, for example.
[0012] As for a digital audio interface circuitry (it consists of ICs for reception/recovery of a digital
audio interface (transmission by the coaxial cable or the optical fiber and a biphase mark use, AES/EBU
specification, or EIAJ standards).), and 2, in drawing 1 and drawing 2 , 1 is [the digital digital disposal
circuit for sound field control and 3] microcomputers. In the digital audio interface circuitry 1, it is the
source signal s1 from sources of a signal, such as CD (compact disk), VD (videodisk), and BS (satellite

broadcasting service). It is inputted and separates into the recognition code (in the case of drawing 1 , in the case of s4 and drawing 2 , it is s4') for identifying a clock signal s2, serial data s3, and a sampling frequency. You may make it input a recognition code (discernment data) into the digital digital disposal circuit 2 for sound field control directly like drawing 1 , and may make it input it into the digital digital disposal circuit 2 for sound field control indirectly through a microcomputer 3 like drawing 2 . The recognition code exists in the code specified in a digital audio interface format, and is beforehand decided to the specific sampling frequency. There are 44.1kHz, 48kHz, and 32kHz in the general sampling frequency used with a digital audio. 44.1kHz It is used with a compact disk, a videodisk, a digital audio tape recorder, etc., and 48kHz / 32kHz are used by the digital audio tape recorder, satellite broadcasting service, etc. The recognition code of three kinds of sampling frequencies may decode these 2 bits with the case where can express by 2 bits and these 2 bits are outputted with two terminals as they are in the digital audio interface circuitry 1, and may output them with three terminals. Digital signal processing is made in the digital digital disposal circuit 2 for sound field control, and the signal-processing result is an output signal s5. It is outputted by carrying out.

[0013] Drawing 3 is the block diagram having shown the configuration of the principal part of the digital digital disposal circuit 2 for sound field control shown in drawing 1 and drawing 2 .

[0014] The multiplier store circuit 4 is two or more sampling frequencies (here, referred to as 1= 44.1kHz of fs(es), 2= 48kHz of fs(es), and 3= 32kHz of fs(es).) about the digital data corresponding to a fixed factor [in / it is constituted using ROM (read-only memory), and / the transfer function of a digital filter] (see the term and drawing 5 of a filter coefficient and the conventional example). In addition, a sampling frequency is equivalent to the frequency of the sampling signal of the A/D-conversion circuit which is not illustrated. It corresponds and memorizes, respectively to two or more storage regions 4a, 4b, and 4c. This multiplier store circuit 4 is constituted from data output section 4e by storage regions 4a, 4b, and 4c and the address decoder 4d list. Each storage regions 4a, 4b, and 4c are specified corresponding to the recognition code s4 (discernment data).

[0015] It is constituted using ROM, C KENSUDE-TA for reading the fixed factor memorized in each storage regions 4a, 4b, and 4c is memorized, and the sequence store circuit 5 is the control signal s6. It is controlled. C KENSUDE-TA s7 And storage region assignment code s8 outputted from the below-mentioned conversion circuit 8 It is inputted into address decoder 4d of the multiplier store circuit 4, and is C KENSUDE-TA s7. To the lower bit of the address, it is the storage region assignment code s8. It becomes a high order bit.

[0016] It is constituted using RAM (random access memory), and the serial data store circuit 6 is the serial data s3 from a digital audio interface circuitry (see drawing 1 and drawing 2). While inputting and memorizing this, the data-processing data s11 from the below-mentioned arithmetic circuit 7 are inputted, and it memorizes.

[0017] An arithmetic circuit 7 is a circuit which performs multiplication and the decrease of addition, and is the fixed factor data s9 from data output section 4e of the multiplier store circuit 4. And in response to the serial data s10 from the serial data store circuit 6, data processing (it is data processing as a digital filter, for example, is data processing corresponding to the formula and drawing 5 which were shown by the term of the conventional example.) is performed, and the result-of-an-operation data s12 is outputted.

[0018] A conversion circuit 8 is the recognition code s4. It encodes or decodes and is the 2-bit storage region assignment code s8. It outputs. storage region assignment code s8 it sets corresponding to each sampling frequencies fs1, fs2, and fs3 -- having -- fs1 -- a code "00" -- f2 **** -- a code "01" -- f3 **** -- a code "10" corresponds, respectively. And at the time of a code "00", storage region 4b is specified at the time of a code "01", and storage region 4c is specified for storage region 4a, respectively at the time of a code "10." Recognition code s4 Storage region assignment code s8 Correspondence relation is the recognition code s4 in the digital audio interface circuitry 1 (see drawing 1 and drawing 2). It changes with output forms (as already stated, these 2 bits may be decoded with the case where a 2-bit recognition code is outputted with two terminals as it is, and it may output with three terminals). When outputting with two terminals, it is the recognition code s4. "00", "01", and "10 or 11" is the storage region

assignment code s8. It corresponds to "00", "01", and "10", respectively. When outputting with three terminals, it is the recognition code s4. "001", "010", and "100" are the storage region assignment code s8. It corresponds to "00", "01", and "10", respectively. A microcomputer 3 is minded like drawing 2 and it is the recognition code s4. When outputted, the above conversion actuation (encoding or decoding) may be performed within a microcomputer 3, and a conversion circuit 8 can be omitted in this case. In addition, the above-mentioned recognition code s4 And storage region assignment code s8 The shown concrete code is a mere example and, of course, expressing in codes other than these is also possible.

[0019] It explains with reference to the flow chart which showed actuation of the example shown in drawing 1 , drawing 2 , and drawing 3 below to drawing 4 . In addition, this flow chart is for explaining the function of a system, makes hardware processing and sequence processing intermingled, and is shown.

[0020] Storage region assignment code s8 which encoded or decoded the recognition code s4 (discernment data) If inputted into address decoder 4d of the multiplier store circuit 4, it will be judged any of "00", "01", and "10" the code is. In fact, these codes are judged by hardware. The fixed factor data s9 (filter multiplier data) corresponding to [when a storage region assignment code is "00", storage region 4a is specified, and] a sampling frequency fs1 are C KENSUDE-TA s7 from the sequence store circuit 5. A sequential output is followed and carried out. Fixed factor data s9 corresponding to [when a storage region assignment code is "01", storage region 4b is specified and] a sampling frequency fs2 It is outputted similarly. Fixed factor data s9 corresponding to [when a storage region assignment code is "10", storage region 4c is specified, and] a sampling frequency fs3 It is outputted similarly. In an arithmetic circuit 7, it is the fixed factor data s9 from the multiplier store circuit 4. And data processing is performed in response to the serial data s10 from the serial data store circuit 6, and the result-of-an-operation data s12 is outputted. It is based on the result-of-an-operation data s12, and, finally is an output signal s5 from the digital digital disposal circuit for sound field control. It is outputted (see drawing 1 and drawing 2 R> 2).

[0021]
[Effect of the Invention] Since it is not necessary to prepare two or more signal processors corresponding to each sampling frequency, the digital digital disposal circuit for sound field control can consist of this inventions, without increasing a hardware scale.

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TECHNICAL FIELD

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control.

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PRIOR ART

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[0003] Since CD (compact disk) appeared in 1982, digital Ore DIOSO-SU is increasing. For example, they are DAT (digital audio tape recorder), BS (satellite broadcasting service), VD (videodisk player), etc. The data transmission between devices is possible for these DEJITARUSO-SU by the digital audio interface. By this, while having a digital input, the amplifier equipped with the D/A conversion circuit has appeared. According to this, compared with what was transmitting the audio signal between devices by the analog transmission, reduction of an external noise and reduction of tone-quality degradation accompanying various kinds of analog signal processings are possible.
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[0006] When it constitutes signal processing systems for sound field control, such as the above-mentioned Dolby prologic decoder, using digital signal processing, there is an IIR (Infinite Impulse Response) digital filter as an operation system which is to the base in the case of performing processing. Hereafter, it explains taking the case of a secondaryIIR filter (BAIKADDO filter). Transfer function of a secondaryIIR filter "H (z)" $H(z) = (a0 + a1*z-1 + a2*z-2)/(1 - b1*z-1 - b2*z-2)$
It becomes. It is here and is z=exp (-jomegaTs).
omega=2pif ("f" is an analog frequency)
Ts =1/fs ("fs" is a sampling frequency)
It is j2 =-1. Moreover, the configuration of this secondaryIIR filter is shown in drawing 5 . As shown in

an upper type, when a sampling frequency "fs" changes, the value of "H (z)" in a certain specific analog frequency will change with change of "z=exp (-jomegaTs)." That is, in order to keep "H (z)" the same to two or more sampling frequencies "fs", each fixed factor (filter factor) "a0" of an upper type, "a1", "a2", "b1", and "b2" must be changed. Therefore, in order [three kinds of] to make it correspond to "fs" (fs1, fs2, fs3) fixed factor corresponding to fs1 : a01, a11, a21, b11, fixed factor corresponding to b21fs2 : a02, a12, a22, b12, fixed factor corresponding to b22fs3 : Three fixed factor sets of a03, a13, a23, b13, and b23 are needed.

[0007] Above, when digital signal processing performs a signal processing system for sound field control like the Dolby prologic decoder currently conventionally performed mainly by analog signal processing, it is necessary to determine a fixed factor (filter factor) like, depending on a sampling frequency. Thus, when performing digital signal processing to two or more sampling frequencies, two or more signal processors are prepared corresponding to each sampling frequency, and, generally the method of switching those equipments according to each sampling frequency, and obtaining an operation output is considered.

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EFFECT OF THE INVENTION

[Effect of the Invention] Since it is not necessary to prepare two or more signal processors corresponding to each sampling frequency, the digital digital disposal circuit for sound field control can consist of this inventions, without increasing a hardware scale.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, by the above-mentioned conventional approach, in
order to have to prepare two or more signal processors corresponding to each sampling frequency, there
was a trouble that the scale of hardware became large.
[0009] In the digital signal processing system for sound field control, the purpose of this invention is
offering the circuit which can be constituted, without increasing a hardware scale, when dealing with
two or more sampling frequencies.

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MEANS

[Means for Solving the Problem] In the digital digital disposal circuit for sound field control which this invention carries out digital data processing of the audio signal of two channels by which the analog to digital was carried out in arithmetic circuits, such as a digital filter, and acquires the digital output signal of three or more channels The digital data corresponding to the fixed factor in the transfer function of a digital filter is memorized to two or more storage regions corresponding to two or more sampling frequencies which can be set in the above-mentioned analog-to-digital actuation. The multiplier store circuit where two or more above-mentioned storage regions are specified corresponding to the discernment data which identify two or more above-mentioned sampling frequencies, C KENSUDE-TA which reads the above-mentioned fixed factor memorized in the above-mentioned storage region is memorized, and it is characterized by having the sequence store circuit which reads the above-mentioned fixed factor by this C KENSUDE-TA.

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EXAMPLE

[Example] Drawing 1 and drawing 2 are the block diagrams having shown the system containing the digital digital·disposal circuit for sound field control. What is necessary is not to·be·limited to this, of course, to carry out digital data processing of the audio signal of two channels by which the analog to digital was carried out in arithmetic circuits, such as a digital filter, and just to acquire the digital output signal of three or more channels as a digital digital disposal circuit for sound field control, although a Dolby prologic decoder (a configuration equivalent to this is constituted in digital one here although the decoder indicated by JP,61-251400,A etc. is said.) can be raised, for example.
[0012] As for a digital audio interface circuitry (it consists of ICs for reception/recovery of a digital audio interface (transmission by the coaxial cable or the optical fiber and a biphase mark use, AES/EBU specification, or EIAJ standards).), and 2, in drawing 1 and drawing 2, 1 is [the digital digital disposal circuit for sound field control and 3] microcomputers. In the digital audio interface circuitry 1, it is the source signal s1 from sources of a signal, such as CD (compact disk), VD (videodisk), and BS (satellite broadcasting service). It is inputted and separates into the recognition code (in the case of drawing 1, in the case of s4 and drawing 2, it is s4') for identifying a clock signal s2, serial data s3, and a sampling frequency. You may make it input a recognition code (discernment data) into the digital digital disposal circuit 2 for sound field control directly like drawing 1, and may make it input it into the digital digital disposal circuit 2 for sound field control indirectly through a microcomputer 3 like drawing 2. The recognition code exists in the code specified in a digital audio interface format, and is beforehand decided to the specific sampling frequency. There are 44.1kHz, 48kHz, and 32kHz in the general sampling frequency used with a digital audio. 44.1kHz It is used with a compact disk, a videodisk, a digital audio tape recorder, etc., and 48kHz / 32kHz are used by the digital audio tape recorder, satellite broadcasting service, etc. The recognition code of three kinds of sampling frequencies may decode these 2 bits with the case where can express by 2 bits and these 2 bits are outputted with two terminals as they are in the digital audio interface circuitry 1, and may output them with three terminals. Digital signal processing is made in the digital digital disposal circuit 2 for sound field control, and the signal-processing result is an output signal s5. It is outputted by carrying out.
[0013] Drawing 3 is the block diagram having shown the configuration of the principal part of the digital digital disposal circuit 2 for sound field control shown in drawing 1 and drawing 2.
[0014] The multiplier store circuit 4 is two or more sampling frequencies (here, referred to as 1= 44.1kHz of fs(es), 2= 48kHz of fs(es), and 3= 32kHz of fs(es).) about the digital data corresponding to a fixed factor [in / it is constituted using ROM (read-only memory), and / the transfer function of a digital filter] (see the term and drawing 5 of a filter coefficient and the conventional example). In addition, a sampling frequency is equivalent to the frequency of the sampling signal of the A/D-conversion circuit which is not illustrated. It corresponds and memorizes, respectively to two or more storage regions 4a, 4b, and 4c. This multiplier store circuit 4 is constituted from data output section 4e by storage regions 4a, 4b, and 4c and the address decoder 4d list. Each storage regions 4a, 4b, and 4c are specified corresponding to the recognition code s4 (discernment data).
[0015] It is constituted using ROM, C KENSUDE-TA for reading the fixed factor memorized in each

storage regions 4a, 4b, and 4c is memorized, and the sequence store circuit 5 is the control signal s6. It is controlled. C KENSUDE-TA s7 And storage region assignment code s8 outputted from the below-mentioned conversion circuit 8 It is inputted into address decoder 4d of the multiplier store circuit 4, and is C KENSUDE-TA s7. To the lower bit of the address, it is the storage region assignment code s8. It becomes a high order bit.

[0016] It is constituted using RAM (random access memory), and the serial data store circuit 6 is the serial data s3 from a digital audio interface circuitry (see drawing 1 and drawing 2). While inputting and memorizing this, the data-processing data s11 from the below-mentioned arithmetic circuit 7 are inputted, and it memorizes.

[0017] An arithmetic circuit 7 is a circuit which performs multiplication and the decrease of addition, and is the fixed factor data s9 from data output section 4e of the multiplier store circuit 4. And in response to the serial data s10 from the serial data store circuit 6, data processing (it is data processing as a digital filter, for example, is data processing corresponding to the formula and drawing 5 which were shown by the term of the conventional example.) is performed, and the result-of-an-operation data s12 is outputted.

[0018] A conversion circuit 8 is the recognition code s4. It encodes or decodes and is the 2-bit storage region assignment code s8. It outputs. storage region assignment code s8 it sets corresponding to each sampling frequencies fs1, fs2, and fs3 -- having -- fs1 -- a code "00" -- f2 **** -- a code "01" -- f3 **** -- a code "10" corresponds, respectively. And at the time of a code "00", storage region 4b is specified at the time of a code "01", and storage region 4c is specified for storage region 4a, respectively at the time of a code "10." Recognition code s4 Storage region assignment code s8 Correspondence relation is the recognition code s4 in the digital audio interface circuitry 1 (see drawing 1 and drawing 2). It changes with output forms (as already stated, these 2 bits may be decoded with the case where a 2-bit recognition code is outputted with two terminals as it is, and it may output with three terminals). When outputting with two terminals, it is the recognition code s4. "00", "01", and "10 or 11" is the storage region assignment code s8. It corresponds to "00", "01", and "10", respectively. When outputting with three terminals, it is the recognition code s4. "001", "010", and "100" are the storage region assignment code s8. It corresponds to "00", "01", and "10", respectively. A microcomputer 3 is minded like drawing 2 and it is the recognition code s4. When outputted, the above conversion actuation (encoding or decoding) may be performed within a microcomputer 3, and a conversion circuit 8 can be omitted in this case. In addition, the above-mentioned recognition code s4 And storage region assignment code s8 The shown concrete code is a mere example and, of course, expressing in codes other than these is also possible.

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[0020] Storage region assignment code s8 which encoded or decoded the recognition code s4 (discernment data) If inputted into address decoder 4d of the multiplier store circuit 4, it will be judged any of "00", "01", and "10" the code is. In fact, these codes are judged by hardware. The fixed factor data s9 (filter multiplier data) corresponding to [when a storage region assignment code is "00", storage region 4a is specified, and] a sampling frequency fs1 are C KENSUDE-TA s7 from the sequence store circuit 5. A sequential output is followed and carried out. Fixed factor data s9 corresponding to [when a storage region assignment code is "01", storage region 4b is specified and] a sampling frequency fs2 It is outputted similarly. Fixed factor data s9 corresponding to [when a storage region assignment code is "10", storage region 4c is specified, and] a sampling frequency fs3 It is outputted similarly. In an arithmetic circuit 7, it is the fixed factor data s9 from the multiplier store circuit 4. And data processing is performed in response to the serial data s10 from the serial data store circuit 6, and the result-of-an-operation data s12 is outputted. It is based on the result-of-an-operation data s12, and, finally is an output signal s5 from the digital digital disposal circuit for sound field control. It is outputted (see drawing 1 and drawing 2 R> 2).

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram having shown the example of this invention.
[Drawing 2] It is the block diagram having shown the example of this invention.
[Drawing 3] It is the block diagram having shown the important section of drawing 1 and drawing 2 .
[Drawing 4] It is the flow chart which showed actuation of drawing 1 , drawing 2 , and drawing 3 .
[Drawing 5] It is the explanatory view having shown data processing of a digital filter.
[Description of Notations]
2 .... Digital digital disposal circuit for sound field control
4 .... Multiplier store circuit
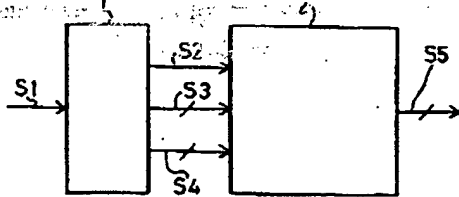5 .... Sequence store circuit

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[Translation done.]

* NOTICES *

JPO and NCIPI are not responsible for any
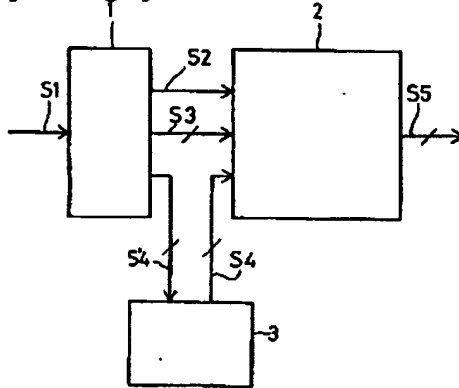damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.
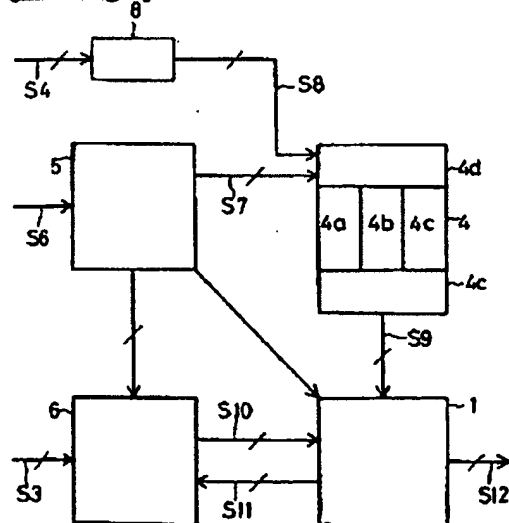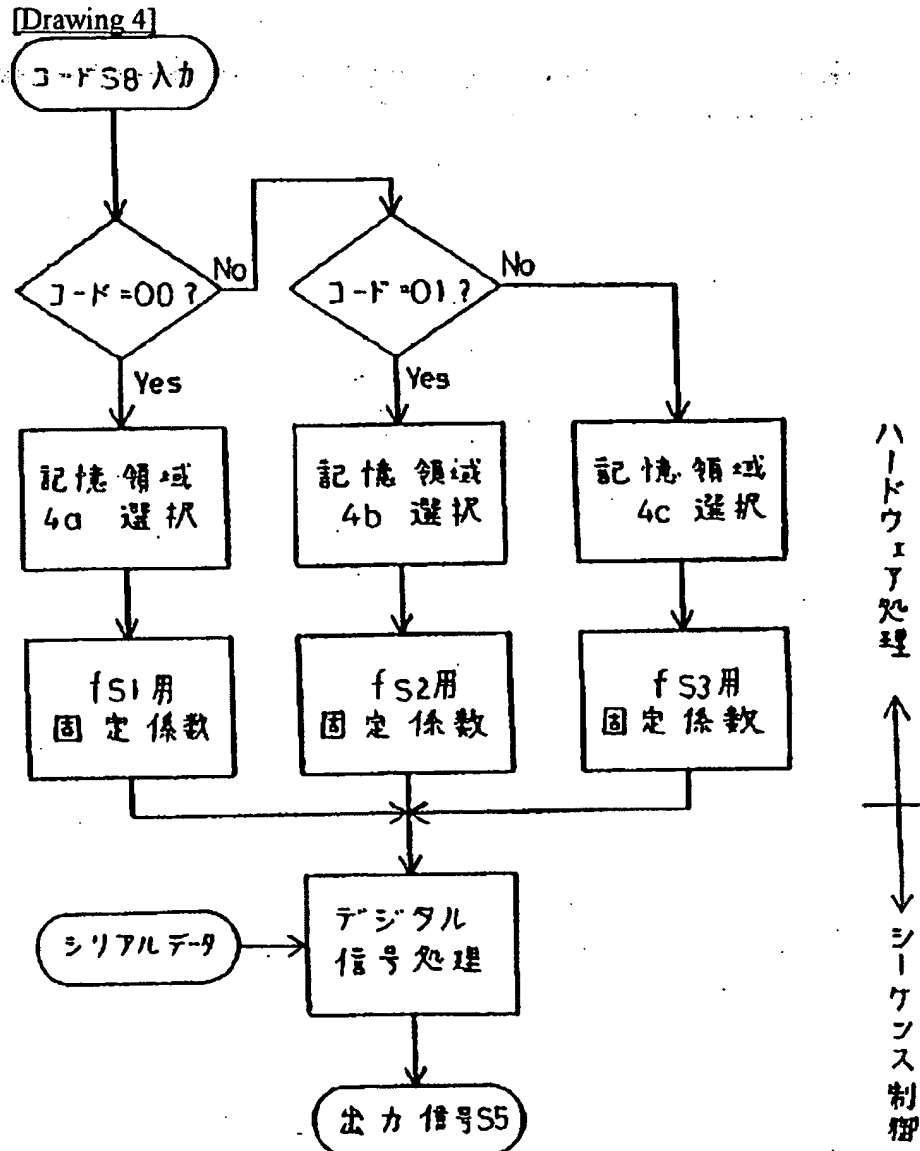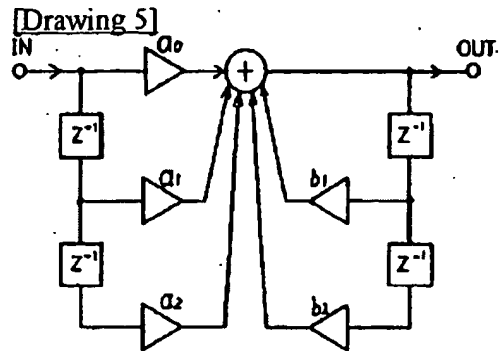

DRAWINGS

[Drawing 1]

[Drawing 2]

[Drawing 3]

[Drawing 5]

IN a_0 OUT

z^{-1} a_1 b_1 z^{-1}

z^{-1} a_2 b_2 z^{-1}

[Drawing 4]

コードS8 入力

コード=00 ？ — No

コード=01 ？ — No

Yes

Yes

記憶領域 4a 選択

記憶領域 4b 選択

記憶領域 4c 選択

fS1用 固定係数

fS2用 固定係数

fS3用 固定係数

シリアルデータ

デジタル 信号処理

出力信号S5

ハードウェア処理

シーケンス制御

[Translation done.]